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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,196	12/04/2001	Jae-Yong Jeong	4591-214	8847

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MARGER JOHNSON & MCCOLLOM PC
1030 SW MORRISON STREET
PORTLAND, OR 97205

EXAMINER
YOHA, CONNIE C

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/006,196	JEONG ET AL.	
	Examiner	Art Unit	
	Connie c. Yoha	2818	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondenc address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-18 and 20-23* is/are rejected.

7)☒ Claim(s) *4, 19, 24 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

Information Disclosure Statement (IDS) filed on 7/16/02 was considered.

2. Claims 1-25 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-3, 5-18, 20-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Arase, Pat. No. 5969990.

With regard to claim 21, Arase discloses a memory cell array (fig. 2, 10) having a plurality of cell strings formed of a string select transistor (fig. 2, ST1) having a drain connected to a bit line (fig. MBLa, MBb) corresponding thereto, a ground select transistor (fig. 2, ST2) having a source connected to a common source line (fig. 2, GND), and a plurality of memory cell transistors (fig. 2, MT1-MT4) serially connected between a source of the string select transistor and a drain of the ground select transistor, word lines (fig. 2, WL1-WL4) connected to control gates of the memory cell

transistors in the respective cell string, a string select line (fig. 2, SL11) commonly connected to gates of the string select transistors in the respective cell string, and a ground select line (fig. 2, SL12) commonly connected to gates of the ground select transistors in the respective cell string; a means (fig. 1, 50) for controlling potentials of the select lines (fig.2, SL11, SL12) and the word lines (fig.2, WL11-WL14) in accordance with a bit line setup, string select line setup, a program, and a discharge period of a program cycle (col. 10, line 62-67); and a page buffer (fig. 1, 30) for supplying a first and second voltage to the bit lines in accordance with the data bits to be programmed in the memory cell array during the bit line setup period of the program cycle, wherein the control means biases the string select line to the first voltage during the bit line setup period and to a third voltage between the first and second voltage during the string select line setup and program periods (col. 12, line 1-46).

With regard to claim 22, Arase discloses wherein the first voltage is a ground voltage, and the second voltage is a power supply voltage (col. 12, line 1-32).

With regard to claim 23, Arase discloses wherein the third voltage is sufficient to turn on the string select transistor connected to the bit line corresponding to the data bit to be programmed (col. 12, line 45-47).

Drafted as Method claim

As per claim 1-3, 5-18, 20 encompass the same scope of invention as to that of claim 21-23 except they draft in method format instead of apparatus format. The claims are therefore rejected for the same reason as set forth above.

Allowabl Subj ct Matt r

4. Claim 4, 19, 24 and 25 are objected as being dependent upon a rejected base claim 1 and 21, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not show the limitation of wherein the third voltage is substantially twice a threshold voltage of NMOS transistor and wherein the third voltage is between a fourth and fifth voltages, wherein the fourth voltage is sufficient to turn on the first select transistor connected to the bit line corresponding to the data bit to be programmed, and wherein the fifth voltage is a shut-off voltage of the first select transistor for the bit line corresponding to the data bit to be program inhibited, the shut-off voltage being determined by the first voltage –(BxVpgm), wherein B is a coupling ratio of the word line to the string select line and wherein Vpgm is the program voltage.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Lee (6480419) and Hirose et al (6163048) disclose a memory device.

6. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 306-5731. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phone number for this Group is (703) 308-7722. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

C. Yoha

May 2003

Connie C. Yoha

Patent Examiner

Art Unit 2818